**WHAT IS CLAIMED IS**:

1. A method of packaging a microelectronic die, comprising:

placing a thermally conductive material on a die substrate; and

establishing thermal contact between an outer region located outside of the inner region and the thermally conductive material placed in the inner region to effect a dissipation of heat away from the die.

2. The method according to claim 1, wherein establishing thermal contact includes:

etching the die substrate to expose thermal contact zones of the thermally conductive material; and

placing a heat dissipation device in thermal contact with the thermal contact zones.

3. A method of packaging a microelectronic die, comprising:

depositing a layer of thermally conductive material on a die substrate;

depositing a layer of dielectric on the layer of thermally conductive material such that the layer of thermally conductive material is placed in an inner region located between the die substrate and the layer of dielectric;

providing a microelectronic circuit the layer of dielectric; and

establishing thermal contact between an outer region located outside of the inner region and the layer of thermally conductive material placed in the inner region to effect a dissipation of heat away from the microelectronic circuit.

4. The method according to claim 3, wherein establishing comprises creating at least one via in the die substrate prior to depositing the layer of thermally conductive material.

5. The method according to claim 4, wherein depositing the layer of thermally conductive material includes depositing some of the thermally conductive material in the at least one via.

6. The method according to claim 3, wherein establishing thermal contact comprises etching the die substrate to expose thermal contact zones of the layer of thermally conductive material.

7. The method according to claim 6, wherein establishing thermal contact comprises:

applying a thermal interface material to the thermal contact zones; and

placing a heat dissipation device in thermal contact with the thermal interface material applied to the thermal contact zones to create a first package and to effect a dissipation of heat away from the microelectronic circuit through the thermal interface material and the heat dissipation device.

8. The method according to claim 7, wherein placing a heat dissipation device comprises attaching the heat dissipation device to the thermal interface material.

9. The method according to claim 8, wherein attaching includes reflowing the first package.

10. The method according to claim 3, further comprising depositing an adhesion promoter on the die substrate before depositing the layer of thermally conductive material to enhance an adhesion of the layer of thermally conductive material to the die substrate.

11. A method of packaging a microelectronic die, comprising:

creating a plurality of vias in a silicon wafer;

depositing a layer of copper on the silicon wafer such that at least some of the copper is deposited in the plurality of vias;

depositing a layer of silicon on the layer of copper such that the layer of copper is placed in an inner region located between the silicon wafer and the layer of silicon;

providing a microelectronic circuit on the layer of silicon; and

establishing thermal contact between an outer region located outside of the inner region and the layer of copper placed in the inner region to effect a dissipation of heat away from the microelectronic circuit, establishing thermal contact including:

etching the silicon wafer to expose a plurality of thermal contact zones of the layer of copper, each of the thermal contact zones corresponding to a location of a respective one of the plurality of vias;

applying solder to each of the thermal contact zones; and

placing a heat dissipation device over the solder to create a first package to effect a dissipation of heat away from the microelectronic circuit through the solder and the heat dissipation device.

12. The method according to claim 11, wherein placing includes attaching the heat dissipation device to the solder by reflowing the first package.

13. A microelectronic die package comprising:

a die substrate;

a layer of dielectric mounted to the die substrate;

a thermally conductive material disposed in an inner region located between the die substrate and the layer of dielectric; and

thermal contact elements disposed between an outer region located outside of the inner region and the thermally conductive material disposed in the inner region to effect a dissipation of heat away from the die.

14. The microelectronic die package according to claim 13, wherein:

the thermally conductive material defines thermal contact zones; and

the thermal contact elements comprise a heat dissipation device in thermal contact with the thermal contact zones.

15. The microelectronic die package according to claim 13, wherein:

the thermally conductive material comprises a layer of thermally conductive material;

the die substrate defines at least one via therein, at least some of the layer of thermally conductive material being located in the at least one via, the at least some of the layer of thermally conductive material further defining the thermal contact zones and being

in thermal contact with the thermal contact elements.

16. The microelectronic die package according to claim 15, wherein the thermal contact elements comprise:

solder in thermal contact with the thermal contact zones; and

a heat dissipation device in thermal contact with the solder.

17. The microelectronic die package according to claim 16, wherein the heat dissipation device is attached to the solder.

18. The microelectronic die package according to claim 13, further comprising an adhesion promoter disposed between the thermally conductive material and the die substrate to enhance an adhesion of the layer of thermally conductive material to the die substrate.

19. A microelectronic die package comprising:

a silicon wafer defining a plurality of vias therein;

a layer of copper on the silicon wafer, at least some of the copper being disposed in the plurality of vias to define thermal contact zones in the plurality of vias;

a layer of silicon disposed on the layer of copper, the layer of copper being disposed in an inner region located between the silicon wafer and the layer of silicon;

a microelectronic circuit provided on the layer of silicon; and

thermal contact elements disposed between an outer region located outside of the inner region and the layer of copper in the inner region to effect a dissipation of heat away

from the microelectronic circuit, the thermal contact zones in the plurality of vias being in thermal contact with the thermal contact elements, the thermal contact elements comprising:

solder in thermal contact with the thermal contact zones in the plurality of vias; and

a heat dissipation device in thermal contact with the solder.

20. The microelectronic die package according to claim 19, wherein the heat dissipation device is attached to the solder.

21. The microelectronic die package according to claim 19, further comprising an adhesion promoter disposed between the layer of copper and the silicon wafer to enhance an adhesion of the copper to the silicon wafer.

22. A thermally conductive microelectronic die substrate for a microelectronic die comprising:

a die substrate; and

a thermally conductive material provided on the die substrate and defining thermal contact zones configured to effect a dissipation of heat away from the die.

23. The thermally conductive microelectronic die substrate according to claim 22, further comprising a layer of dielectric mounted to the die substrate, the thermally conductive material being disposed in an inner region between the die substrate and the layer of dielectric.

24. The thermally conductive microelectronic die substrate according to claim 23, wherein:

the die substrate comprises a silicon wafer;

the layer of dielectric comprises a layer of silicon mounted to the silicon wafer; and

the thermally conductive material comprises a layer of copper in the inner region, the silicon wafer further defining at least one via therein, and some of the layer of copper being disposed in the at least one via to define the thermal contact zones.

25. A microelectronic die package comprising:

a die substrate;

a layer of dielectric mounted to the die substrate;

means disposed in an inner region located between the die substrate and the layer of dielectric for effecting a dissipation of heat away from the microelectronic circuit; and

means in thermal contact with the means for effecting for directing heat away from the die through the means for effecting.

26. The die according to claim 25, wherein the means for effecting comprises a layer of copper.

27. The die according to claim 25, wherein the means for directing comprises a heat dissipation device.